SAMSUNG

ARTIK™ Modules

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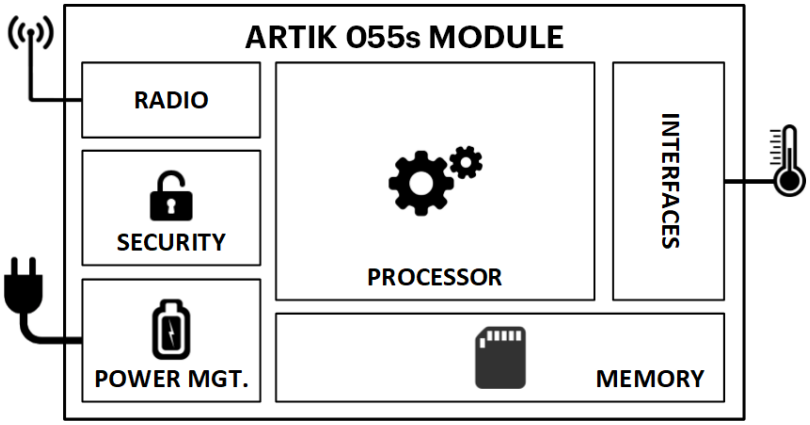
ARTIK 055s Module Datasheet

Module Overview

Figure 1. ARTIK 055s Module Top View

The Samsung ARTIK™ 055s Module is a highly integrated module for secure Internet of Things (IoT) devices that require Wi-Fi® connectivity. It is based on an ARM® Cortex® R4 core, with on-module RAM and flash memory, a complete 2.4GHz Wi-Fi subsystem with on-module antenna, an independent security subsystem, PUF-based module authentication, and a large complement of standard I/O interfaces.

The ARTIK 055s Module provides excellent performance in a variety of environments, with a feature set tailored specifically for IoT end nodes.



Processor	
CPU	32-bit ARM® Cortex® R4 with 32KB I-Cache and 32KB D-Cache @ 320MHz
Memory	
RAM	1280KB (General usage) 128KB (Global IPC data)
FLASH	8MB Flash
Security	
Secure Subsystem	AES/DES/TDES, SHA-1/SHA-2, PKA (Public Key Accelerator), PRNG/DTRNG (Random Number Generators), Secure key storage
PUF	Physically Unclonable Function
Radio	
Wi-Fi	Certified IEEE802.11™ b/g/n Wi-Fi® 2.4GHz radio served by a dedicated 32-bit ARM Cortex R4 with 32KB I-Cache and 16KB D-Cache @ 480MHz
Regulatory	FCC (U.S.), IC (Canada), CE (EU), KC (Korea), SRRC (China)
Power Management	
Single Supply	3.3V
Interfaces	
I/O	UART, I^2C, SPI, PWM, ADC, GPIO. I^2S
Form Factor	
Dimensions	15mm W x 26mm D x 3.9mm H
Operation Enviroment	
Temperture	–20 to 85 ^oC T_c

Table of Contents

List of Figures

List of Tables

VERSION HISTORY

Revision	Date	Description
V1.0	November 20, 2017	First release.
V1.1	November 30, 2017	Modified GPIO name for XSPI1_MISO,XSPI1_MOSI, XSPI1_CLK, and XSPI1_CSN in *Table 1* and *Table 4* to be consistent with assigned name in *Table 2*. Removed GPIO names from *Table 9*. Added maximum storage temperature range, T_A, in *Absolute Maximum Rating* section.
V1.2	December 6, 2017	Updated *Mechanical Specifications*.
V1.3	January 8, 2018	*SRRC*: Updated CMIIT ID. *Wi-Fi*: Certification information and certification ID added.
V1.4	January 10, 2018	*Module Antenna Placement Requirements*: Modified and separated PCB routing and component placement keep-out areas. *I^2S Interface*: Changed features to indicate that the interface operates in slave mode only.

Block Diagram

Figure 2 shows a functional block diagram of the ARTIK 055s Module.

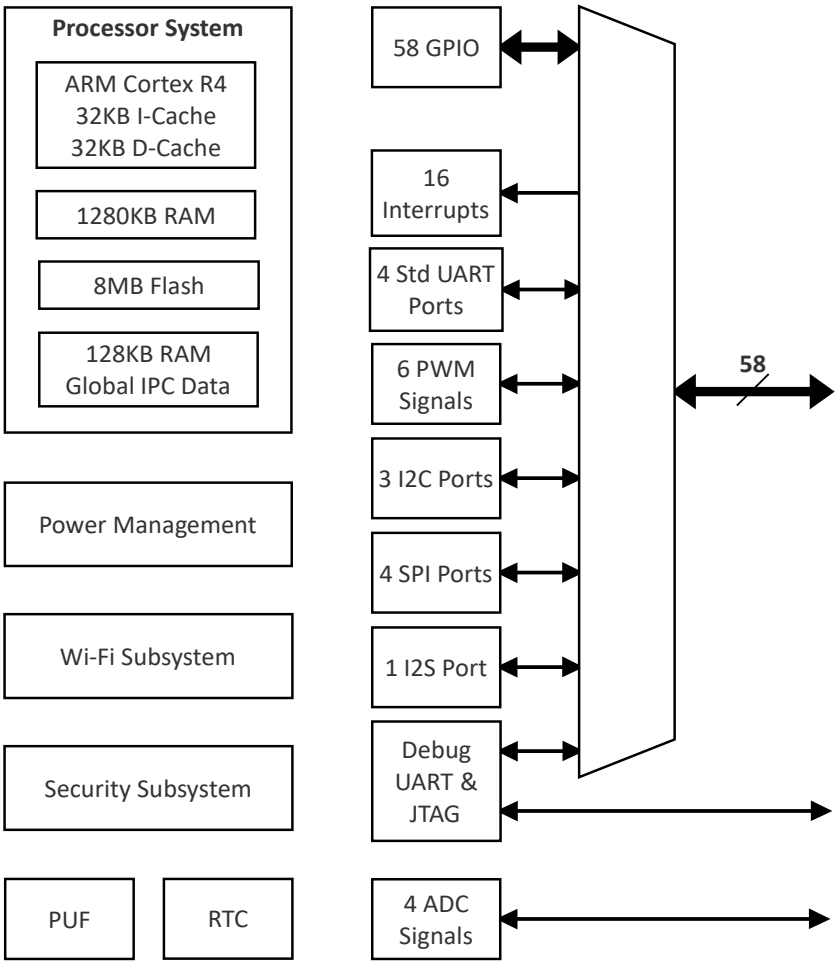


Figure 2. ARTIK 055s Module Block Diagram

CPU

The ARTIK 055s Module CPU has an ARM® Cortex® R4. It has the following features:

- 32KB of Instruction Cache (I-Cache)
- 32KB of Data Cache (D-Cache)
- 320MHz execution clock
- R4 core tuned for embedded and real-time applications

Memory

The ARTIK 055s Module on-module memory has the following features:

- CPU and general purpose RAM
  - 1280KB CPU RAM
  - 128KB global Inter-Process Communication (IPC) RAM
- 8MB flash

Real Time Clock

The ARTIK 055s Module has a Real Time Clock (RTC) for tracking date/time. The RTC has the following features:

- Binary-Coded Decimal (BCD) coded seconds, minutes, hour, day of the week, day, month, and year
- Leap year detection and compensation
- Millisecond tick time interrupt for Real-Time Operating System (RTOS) kernel time tick

PUF Unit

The ARTIK 055s Module has a Physically Unclonable Function (PUF) unit. The PUF unit has the following features:

- Generates unique key values, locked to an individual ARTIK 055s Module
- The algorithm construction is unique to each module
- Allows individual ARTIK 055s Modules to be “fingerprint-identified”

Security Subsystem

The ARTIK 055s Module has an independent security subsystem to ensure secure end-to-end operation in any IoT environment. The security subsystem includes the following features:

- Secure IPC Mailbox for inter-subsystem communication
- Encapsulated key support
  - Backup encryption key - 256 bits
  - Security subsystem root private key - 521 bits
  - Storage key - 256 bits
- Symmetric key engines
  - Secure AES
  - Secure DES/Triple-DES
- Stream cipher engine
  - ARC4 engine
- Various Hash engines
  - SHA-1, SHA2-256, SHA2-384, SHA2-512, MD5 HMAC
- Asymmetric key engines
  - PKA (Public Key Accelerator) engine
- PRNG (Pseudo Random Number Generator)
- DTRNG (Digital True Random Number Generator)
- Secure key storage

Wi-Fi Subsystem

The ARTIK 055s Module has an 802.11b/g/n Wi-Fi subsystem. The Wi-Fi subsystem has the following features:

- 802.11™ b/g/n support at 2.4GHz
- 20MHz single stream (802.11n)
- WPA/WPA2
- Dedicated Wi-Fi Processor subsystem with 480MHz 32-bit ARM Cortex R4 supported by 32KB I-Cache and 16KB D-Cache.

GPIO Interfaces

The ARTIK 055s Module has flexible General Purpose Input Output (GPIO) interfaces:

- 58 configurable GPIO ports
- Independently configurable for either general purpose input or output
- 43 configurable for alternate functionality
- Configurable internal pull-up or pull-down resistors

SPI Interfaces

The ARTIK 055s Module has four SPI interfaces, each with the following features:

- Full duplex communication
- 8, 16 or 32-bit shift registers and bus interface
- Motorola SPI protocol and National Semiconductor Microwire protocol
- Master and slave mode operation
- Two independent 32-bit wide transmit/receive FIFOs
- Transmit and receive speeds up to 50MHz

I^2C Interfaces

The ARTIK 055s Module has three high speed multi-master I^2C interfaces available, with speeds up to 3.4Mbps.

PWM Interfaces

The ARTIK 055s Module has six PWM timers, each with the following features:

- 32 bits of resolution for each PWM signal
- Two 8-bit prescalers (first level of division) and 5 clock dividers/multiplexers for second-level division
- Continuous run or one-shot pulse mode
- Dead zone generator to avoid simultaneous change of multiple PWM signals
- Interrupt generation

I²S Interface

The ARTIK 055s Module has one I²S interface with the following features:

- Each channel includes a 32-bit × 64 data FIFO for both transmit and receive
- Supports stereo I²S bus channels with external DMA-based operations
- Can mix two sound sources from a primary and secondary source
- Serial data transfer formats of 8 bits, 16 bits, or 24 bits per channel
- Supports both MSB and LSB justified data formats
- Operates in I²S slave mode only

ADC Interfaces

The ARTIK 055s Module has four analog-to-digital converter (ADC) channels. Each interface has the following features:

- 12-bit resolution
- ADC conversion clock at 1.08 mega-samples per second (MSPS) using a main 6.5MHz clock
- Supports sample averaging over 1, 2, 4, 8, 16, 32, or 64 samples
- Differential non-linearity error range of ±2 LSB bits (value of ±2)
- Integral non-linearity error range of ±3 LSB bits (value of ±6)
- Top and bottom offset error range of ±4 LSB bits (value of ±10)
- Voltage range up to 1.8V

Figure 3 depicts the dynamic behavior between input voltage on the ADC and resulting LSB value in the ADC register.

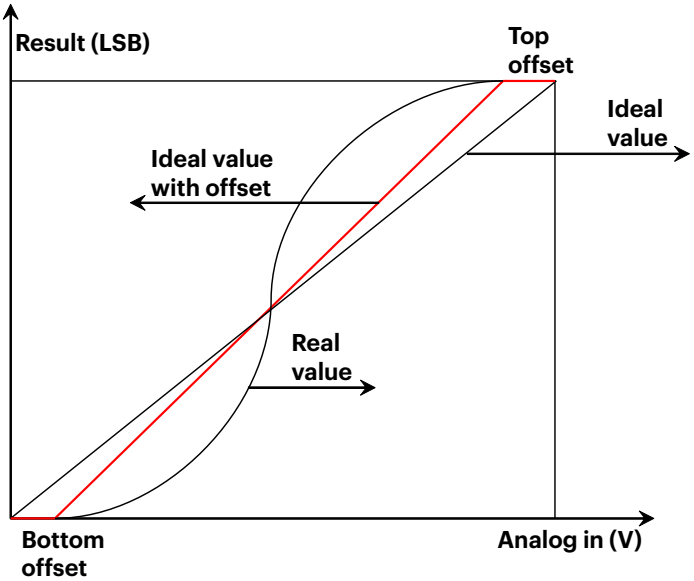


Figure 3. ADC LSB behavior

UART Interfaces

The ARTIK 055s Module has five 2-pin UART interfaces; one is used in the debug block. Each has the following features:

- Can be operated in DMA or interrupt-based mode
- Support for 5, 6, 7, or 8-bit serial data transmit and receive
- Programmable baud rate
- One or two stop-bit insertion

Module Pad Physical Layout

The ARTIK 055s Module utilizes 82 signal, power, and ground pads. The figure below shows how the physical layout orients the signal pads assigned at the edge of the ARTIK 055s Module. *Figure 1* shows the edge pads and the signal names.

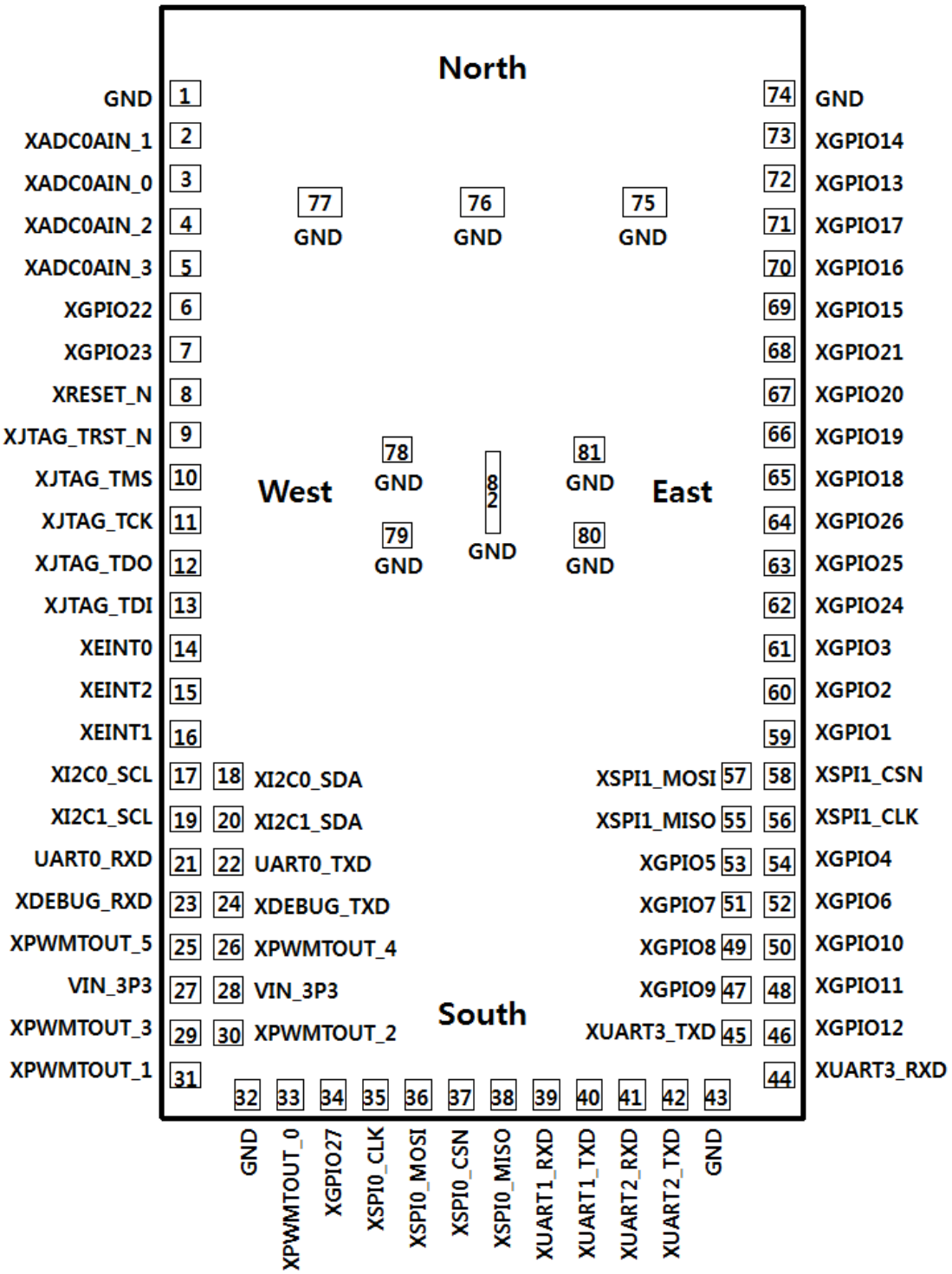


Figure 4. ARTIK 055s Module Edge Pinout (Top View)

Module Pad Signal Definitions

The tables below describes the characteristics of the ARTIK 055s Module pad signals. Some signals can be configured for alternate functionality. The remaining signals have dedicated functionality. Refer to the following column definitions.

- **Pad Number** defines the signal pad on the edge of the module. Refer to *Figure 4* for pad/signal physical layout.
- **Pad Name** defines the net list name of the signal. The pad name may reflect on one of the possible optional signal functionality, and dictates the default power-on function.
- **GPIO Name** defines a generic name for referring to GPIO signals regardless of their current configured functionality. The name order is the same order as the GPIO signals appear in the GPIO configuration registers.
- **PU/PD** defines the power-on state of the internal pull up/pull down definition. PU:pull up, PD:pull down, N:no pull up/down.
- **GPIO Drive** defines the power-on state drive strength of GPIO and other signals. Configurable to 2mA, 4mA, 8mA, or 12mA. Do not use GPIO signals to power discrete components directly (such as LEDs). Use an external driver device instead (such as a transistor).
- **Option 1 - Option 6** lists the alternative functionality some signals can be configured to. Those signals without any options are dedicated to their function. The pad name signifies the default power-on state.

Table 1. ARTIK 055s Module Pinout Signal Descriptions

Pad Number	Pad Name & Default Function	GPIO Name	PU/PD	GPIO Drive	Option 1	Option 2	Option 3	Option 4	Option 5	Option 6
1	GND	–	–	–	–	–	–	–	–	–
2	XADC0AIN_1	–	–	–	–	–	–	–	–	–
3	XADC0AIN_0	–	–	–	–	–	–	–	–	–
4	XADC0AIN_2	–	–	–	–	–	–	–	–	–
5	XADC0AIN_3	–	–	–	–	–	–	–	–	–
6	XGPIO22	GPIO39	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[6]
7	XGPIO23	GPIO40	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[7]
8	XRESET_N	–	–	–	–	–	–	–	–	–
9	XJTAG_TRST_N	–	PD	–	–	–	–	–	–	–
10	XJTAG_TMS	–	PU	–	–	–	–	–	–	–
11	XJTAG_TCK	–	PD	–	–	–	–	–	–	–
12	XJTAG_TDO	–	PD	2mA	–	–	–	–	–	–
13	XJTAG_TDI	–	PU	–	–	–	–	–	–	–
14	XEINT_0	GPIO45	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPA0[0]
15	XEINT_2	GPIO47	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPA0[2]
16	XEINT_1	GPIO46	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPA0[1]
17	XI2C0_SCL	GPIO48	PD	8mA	GP Input	GP Output	HSI2C_0_SCL	–	–	–
18	XI2C0_SDA	GPIO49	PD	8mA	GP Input	GP Output	HSI2C_0_SDA	–	–	–
19	XI2C1_SCL	GPIO50	PD	8mA	GP Input	GP Output	HSI2C_1_SCL	–	–	–
20	XI2C1_SDA	GPIO51	PD	8mA	GP Input	GP Output	HSI2C_1_SDA	–	–	–
21	XUART0_RXD	GPIO52	PD	8mA	GP Input	GP Output	UART_0_RXD	–	–	–
22	XUART0_TXD	GPIO53	PD	8mA	GP Input	GP Output	UART_0_TXD	–	–	–
23	XDEBUG_RXD	GPIO54	PD	8mA	GP Input	GP Output	Xdebug_RXD	–	–	–
24	XDEBUG_TXD	GPIO55	PD	8mA	GP Input	GP Output	Xdebug_TXD	–	–	–
25	XPWMTOUT_5	GPIO16	PD	8mA	GP Input	GP Output	PWM_TOUT_6	–	–	–

Table 1. ARTIK 055s Module Pinout Signal Descriptions (Continued)

Pad Number	Pad Name & Default Function	GPIO Name	PU/PD	GPIO Drive	Option 1	Option 2	Option 3	Option 4	Option 5	Option 6
26	XPWMTOUT_4	GPIO15	PD	8mA	GP Input	GP Output	PWM_TOUT_5	–	–	–
27	VIN_3P3	–	–	–	–	–	–	–	–	–
28	VIN_3P3	–	–	–	–	–	–	–	–	–
29	XPWMTOUT_3	GPIO13	PD	8mA	GP Input	GP Output	PWM_TOUT_3	–	–	–
30	XPWMTOUT_2	GPIO12	PD	8mA	GP Input	GP Output	PWM_TOUT_2	–	–	–
31	XPWMTOUT_1	GPIO11	PD	8mA	GP Input	GP Output	PWM_TOUT_1	COUNTER_0	UART_3_RTSn	–
32	GND	-	–	–	–	–	–	–	–	–
33	XPWMTOUT_0	GPIO10	PD	8mA	GP Input	GP Output	PWM_TOUT_0	–	UART_3_CTSn	–
34	XGPIO27	GPIO44	PD	2mA	GP Input	GP Output	I2S_0_SDI	–	–	–
35	XSPI0_CLK	GPIO00	PD	8mA	GP Input	GP Output	SPI_0_CLK	–	–	–
36	XSPI0_MOSI	GPIO03	PD	8mA	GP Input	GP Output	SPI_0_MOSI	–	–	–
37	XSPI0_CSN	GPIO01	PD	8mA	GP Input	GP Output	SPI_0_CSn	–	–	–
38	XSPI0_MISO	GPIO02	PD	8mA	GP Input	GP Output	SPI_0_MISO	–	–	–
39	XUART1_RXD	GPIO04	PD	8mA	GP Input	GP Output	UART_1_RXD	UART_2_CTSn	–	–
40	XUART1_TXD	GPIO05	PD	8mA	GP Input	GP Output	UART_1_TXD	UART_2_RTSn	–	–
41	XUART2_RXD	GPIO06	PD	8mA	GP Input	GP Output	UART_2_RXD	–	–	–
42	XUART2_TXD	GPIO07	PD	8mA	GP Input	GP Output	UART_2_TXD	–	–	–
43	GND	-	–	–	–	–	–	–	–	–
44	XUART3_RXD	GPIO08	PD	8mA	GP Input	GP Output	UART_3_RXD	–	–	–
45	XUART3_TXD	GPIO09	PD	8mA	GP Input	GP Output	UART_3_TXD	–	–	–
46	XGPIO12	GPIO29	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG1[4]
47	XGPIO9	GPIO26	PD	2mA	GP Input	GP Output	SPI_3_CSn	–	–	NWEINT_GPG1[1]
48	XGPIO11	GPIO28	PD	2mA	GP Input	GP Output	SPI_3_MOSI	–	–	NWEINT_GPG1[3]
49	XGPIO8	GPIO25	PD	2mA	GP Input	GP Output	SPI_3_CLK	–	–	NWEINT_GPG1[0]
50	XGPIO10	GPIO27	PD	2mA	GP Input	GP Output	SPI_3_MISO	–	–	NWEINT_GPG1[2]
51	XGPIO7	GPIO24	PD	2mA	GP Input	GP Output	SPI_2_MOSI	–	–	–
52	XGPIO6	GPIO23	PD	2mA	GP Input	GP Output	SPI_2_MISO	–	–	–
53	XGPIO5	GPIO22	PD	2mA	GP Input	GP Output	SPI_2_CSn	–	–	–
54	XGPIO4	GPIO21	PD	2mA	GP Input	GP Output	SPI_2_CLK	–	–	–
55	XSPI1_MISO	GPIO56	PD	2mA	GP Input	GP Output	SPI_1_MISO	–	–	–
56	XSPI1_CLK	GPIO54	PD	2mA	GP Input	GP Output	SPI_1_CLK	–	–	–
57	XSPI1_MOSI	GPIO57	PD	2mA	GP Input	GP Output	SPI_1_MOSI	–	–	–
58	XSPI1_CSN	GPIO55	PD	2mA	GP Input	GP Output	SPI_1_CSn	–	–	–
59	XGPIO1	GPIO18	PD	2mA	GP Input	GP Output	HSI2C_2_SDA	–	–	–
60	XGPIO2	GPIO19	PD	2mA	GP Input	GP Output	HSI2C_3_SCL	–	–	–
61	XGPIO3	GPIO20	PD	2mA	GP Input	GP Output	HSI2C_3_SDA	–	–	–
62	XGPIO24	GPIO41	PD	2mA	GP Input	GP Output	I2S_0_BCLK	–	–	–
63	XGPIO25	GPIO42	PD	2mA	GP Input	GP Output	I2S_0_LRCK	–	–	–
64	XGPIO26	GPIO43	PD	2mA	GP Input	GP Output	I2S_0_SDO	–	–	–
65	XGPIO18	GPIO35	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[2]
66	XGPIO19	GPIO36	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[3]
67	XGPIO20	GPIO37	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[4]
68	XGPIO21	GPIO38	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[5]
69	XGPIO15	GPIO32	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG1[7]
70	XGPIO16	GPIO33	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[0]
71	XGPIO17	GPIO34	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[1]
72	XGPIO13	GPIO30	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG1[5]
73	XGPIO14	GPIO31	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG1[6]

Table 1. ARTIK 055s Module Pinout Signal Descriptions (Continued)

Pad Number	Pad Name & Default Function	GPIO Name	PU/PD	GPIO Drive	Option 1	Option 2	Option 3	Option 4	Option 5	Option 6
74	GND	–	–	–	–	–	–	–	–	–
75	GND	–	–	–	–	–	–	–	–	–
76	GND	–	–	–	–	–	–	–	–	–
77	GND	–	–	–	–	–	–	–	–	–
78	GND	–	–	–	–	–	–	–	–	–
79	GND	–	–	–	–	–	–	–	–	–
80	GND	–	–	–	–	–	–	–	–	–
81	GND	–	–	–	–	–	–	–	–	–
82	GND	–	–	–	–	–	–	–	–	–

Module Pad Signal Definitions by Function

GPIO Interface

Table 2. GPIO Interface

GPIO Name	Pad Name & Default Function	Pad Number	PU/PD	GPIO Drive	Option 1	Option 2	Option 3	Option 4	Option 5	Option 6
GPIO00	XSPI0_CLK	35	PD	8mA	GP Input	GP Output	SPI_0_CLK	–	–	–
GPIO01	XSPI0_CSN	37	PD	8mA	GP Input	GP Output	SPI_0_CSn	–	–	–
GPIO02	XSPI0_MISO	38	PD	8mA	GP Input	GP Output	SPI_0_MISO	–	–	–
GPIO03	XSPI0_MOSI	36	PD	8mA	GP Input	GP Output	SPI_0_MOSI	–	–	–
GPIO04	XUART1_RXD	39	PD	8mA	GP Input	GP Output	UART_1_RXD	UART_2_CTSn	–	–
GPIO05	XUART1_TXD	40	PD	8mA	GP Input	GP Output	UART_1_TXD	UART_2_RTSn	–	–
GPIO06	XUART2_RXD	41	PD	8mA	GP Input	GP Output	UART_2_RXD	–	–	–
GPIO07	XUART2_TXD	42	PD	8mA	GP Input	GP Output	UART_2_TXD	–	–	–
GPIO08	XUART3_RXD	44	PD	8mA	GP Input	GP Output	UART_3_RXD	–	–	–
GPIO09	XUART3_TXD	45	PD	8mA	GP Input	GP Output	UART_3_TXD	–	–	–
GPIO10	XPWMTOUT_0	33	PD	8mA	GP Input	GP Output	PWM_TOUT_0	–	UART_3_CTSn	–
GPIO11	XPWMTOUT_1	31	PD	8mA	GP Input	GP Output	PWM_TOUT_1	COUNTER_0	UART_3_RTSn	–
GPIO12	XPWMTOUT_2	30	PD	8mA	GP Input	GP Output	PWM_TOUT_2	–	–	–
GPIO13	XPWMTOUT_3	29	PD	8mA	GP Input	GP Output	PWM_TOUT_3	–	–	–
GPIO15	XPWMTOUT_4	26	PD	8mA	GP Input	GP Output	PWM_TOUT_5	–	–	–
GPIO16	XPWMTOUT_5	25	PD	8mA	GP Input	GP Output	PWM_TOUT_6	–	–	–
GPIO18	XGPIO1	59	PD	2mA	GP Input	GP Output	HSI2C_2_SDA	–	–	–
GPIO19	XGPIO2	60	PD	2mA	GP Input	GP Output	HSI2C_3_SCL	–	–	–
GPIO20	XGPIO3	61	PD	2mA	GP Input	GP Output	HSI2C_3_SDA	–	–	–
GPIO21	XGPIO4	54	PD	2mA	GP Input	GP Output	SPI_2_CLK	–	–	–
GPIO22	XGPIO5	53	PD	2mA	GP Input	GP Output	SPI_2_CSn	–	–	–
GPIO23	XGPIO6	52	PD	2mA	GP Input	GP Output	SPI_2_MISO	–	–	–
GPIO24	XGPIO7	51	PD	2mA	GP Input	GP Output	SPI_2_MOSI	–	–	–
GPIO25	XGPIO8	49	PD	2mA	GP Input	GP Output	SPI_3_CLK	–	–	NWEINT_GPG1[0]
GPIO26	XGPIO9	47	PD	2mA	GP Input	GP Output	SPI_3_CSn	–	–	NWEINT_GPG1[1]
GPIO27	XGPIO10	50	PD	2mA	GP Input	GP Output	SPI_3_MISO	–	–	NWEINT_GPG1[2]
GPIO28	XGPIO11	48	PD	2mA	GP Input	GP Output	SPI_3_MOSI	–	–	NWEINT_GPG1[3]
GPIO29	XGPIO12	46	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG1[4]
GPIO30	XGPIO13	72	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG1[5]
GPIO31	XGPIO14	73	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG1[6]
GPIO32	XGPIO15	69	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG1[7]
GPIO33	XGPIO16	70	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[0]
GPIO34	XGPIO17	71	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[1]
GPIO35	XGPIO18	65	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[2]
GPIO36	XGPIO19	66	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[3]
GPIO37	XGPIO20	67	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[4]
GPIO38	XGPIO21	68	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[5]
GPIO39	XGPIO22	6	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[6]
GPIO40	XGPIO23	7	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[7]

Table 2. GPIO Interface (Continued)

GPIO Name	Pad Name & Default Function	Pad Number	PU/PD	GPIO Drive	Option 1	Option 2	Option 3	Option 4	Option 5	Option 6
GPIO41	XGPIO24	62	PD	2mA	GP Input	GP Output	I2S_0_BCLK	–	–	–
GPIO42	XGPIO25	63	PD	2mA	GP Input	GP Output	I2S_0_LRCK	–	–	–
GPIO43	XGPIO26	64	PD	2mA	GP Input	GP Output	I2S_0_SDO	–	–	–
GPIO44	XGPIO27	34	PD	2mA	GP Input	GP Output	I2S_0_SDI	–	–	–
GPIO45	XEINT_0	14	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPA0[0]
GPIO46	XEINT_1	16	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPA0[1]
GPIO47	XEINT_2	15	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPA0[2]
GPIO48	XI2C0_SCL	17	PD	8mA	GP Input	GP Output	HSI2C_0_SCL	–	–	–
GPIO49	XI2C0_SDA	18	PD	8mA	GP Input	GP Output	HSI2C_0_SDA	–	–	–
GPIO50	XI2C1_SCL	19	PD	8mA	GP Input	GP Output	HSI2C_1_SCL	–	–	–
GPIO51	XI2C1_SDA	20	PD	8mA	GP Input	GP Output	HSI2C_1_SDA	–	–	–
GPIO52	XUART0_RXD	21	–	8mA	GP Input	GP Output	UART_0_RXD	–	–	–
GPIO53	XUART0_TXD	22	–	8mA	GP Input	GP Output	UART_0_TXD	–	–	–
GPIO54	XSPI1_CLK	56	PD	2mA	GP Input	GP Output	SPI_1_CLK	–	–	–
GPIO55	XSPI1_CSN	58	PD	2mA	GP Input	GP Output	SPI_1_CSn	–	–	–
GPIO56	XSPI1_MISO	55	PD	2mA	GP Input	GP Output	SPI_1_MISO	–	–	–
GPIO57	XSPI1_MOSI	57	PD	2mA	GP Input	GP Output	SPI_1_MOSI	–	–	–

I^2C Interface

Table 3. I^2C Interface

Pad Name & Default Function	Pad Number	GPIO Name	PU/PD	GPIO Drive	Option 1	Option 2	Option 3	Option 4	Option 5	Option 6
XI2C0_SCL	17	GPIO48	PD	8mA	GP Input	GP Output	HSI2C_0_SCL	–	–	–
XI2C0_SDA	18	GPIO49	PD	8mA	GP Input	GP Output	HSI2C_0_SDA	–	–	–
XI2C1_SCL	19	GPIO50	PD	8mA	GP Input	GP Output	HSI2C_1_SCL	–	–	–
XI2C1_SDA	20	GPIO51	PD	8mA	GP Input	GP Output	HSI2C_1_SDA	–	–	–
XGPIO2	60	GPIO02	PD	2mA	GP Input	GP Output	HSI2C_3_SCL	–	–	–
XGPIO3	61	GPIO03	PD	2mA	GP Input	GP Output	HSI2C_3_SDA	–	–	–

SPI Interface

Table 4. SPI Interface

Pad Name & Default Function	Pad Number	GPIO Name	PU/PD	GPIO Drive	Option 1	Option 2	Option 3	Option 4	Option 5	Option 6
XSPI0_CLK	35	GPIO00	PD	8mA	GP Input	GP Output	SPI_0_CLK	–	–	–
XSPI0_CSN	37	GPIO01	PD	8mA	GP Input	GP Output	SPI_0_CSn	–	–	–
XSPI0_MISO	38	GPIO02	PD	8mA	GP Input	GP Output	SPI_0_MISO	–	–	–
XSPI0_MOSI	36	GPIO03	PD	8mA	GP Input	GP Output	SPI_0_MOSI	–	–	–

Table 4. SPI Interface

Pad Name & Default Function	Pad Number	GPIO Name	PU/PD	GPIO Drive	Option 1	Option 2	Option 3	Option 4	Option 5	Option 6
XSPI1_CLK	56	GPIO54	PD	2mA	GP Input	GP Output	SPI_1_CLK	–	–	–
XSPI1_CSN	58	GPIO55	PD	2mA	GP Input	GP Output	SPI_1_CSn	–	–	–
XSPI1_MISO	55	GPIO56	PD	2mA	GP Input	GP Output	SPI_1_MISO	–	–	–
XSPI1_MOSI	57	GPIO57	PD	2mA	GP Input	GP Output	SPI_1_MOSI	–	–	–
XGPIO5	53	GPIO22	PD	2mA	GP Input	GP Output	SPI_2_CSn	–	–	–
XGPIO4	54	GPIO21	PD	2mA	GP Input	GP Output	SPI_2_CLK	–	–	–
XGPIO6	52	GPIO23	PD	2mA	GP Input	GP Output	SPI_2_MISO	–	–	–
XGPIO7	51	GPIO24	PD	2mA	GP Input	GP Output	SPI_2_MOSI	–	–	–
XGPIO9	47	GPIO26	PD	2mA	GP Input	GP Output	SPI_3_CSn	–	–	NWEINT_GPG1[1]
XGPIO11	48	GPIO28	PD	2mA	GP Input	GP Output	SPI_3_MOSI	–	–	NWEINT_GPG1[3]
XGPIO8	49	GPIO25	PD	2mA	GP Input	GP Output	SPI_3_CLK	–	–	NWEINT_GPG1[0]
XGPIO10	50	GPIO27	PD	2mA	GP Input	GP Output	SPI_3_MISO	–	–	NWEINT_GPG1[2]

I^2S Interface

Table 5. I^2S Interface

Pad Name & Default Function	Pad Number	GPIO Name	PU/PD	GPIO Drive	Option 1	Option 2	Option 3	Option 4	Option 5	Option 6
XGPIO24	62	GPIO41	PD	2mA	GP Input	GP Output	I2S_0_BCLK	–	–	–
XGPIO25	63	GPIO42	PD	2mA	GP Input	GP Output	I2S_0_LRCK	–	–	–
XGPIO26	64	GPIO43	PD	2mA	GP Input	GP Output	I2S_0_SDO	–	–	–
XGPIO27	34	GPIO44	PD	2mA	GP Input	GP Output	I2S_0_SDI	–	–	–

ADC Interface

Table 6. ADC Interface

Pad Name & Default Function	Pad Number	GPIO Name	PU/PD	GPIO Drive	Option 1	Option 2	Option 3	Option 4	Option 5	Option 6
XADC0AIN_0	3	–	–	–	–	–	–	–	–	–
XADC0AIN_1	2	–	–	–	–	–	–	–	–	–
XADC0AIN_2	4	–	–	–	–	–	–	–	–	–
XADC0AIN_3	5	–	–	–	–	–	–	–	–	–

PWM Interface

Table 7. PWM Interface

Pad Name & Default Function	Pad Number	GPIO Name	PU/PD	GPIO Drive	Option 1	Option 2	Option 3	Option 4	Option 5	Option 6
XPWMTOUT_0	33	GPIO10	PD	8mA	GP Input	GP Output	PWM_TOUT_0	–	UART_3_CTSn	–
XPWMTOUT_1	31	GPIO11	PD	8mA	GP Input	GP Output	PWM_TOUT_1	COUNTER_0	UART_3_RTSn	–
XPWMTOUT_2	30	GPIO12	PD	8mA	GP Input	GP Output	PWM_TOUT_2	–	–	–
XPWMTOUT_3	29	GPIO13	PD	8mA	GP Input	GP Output	PWM_TOUT_3	–	–	–
XPWMTOUT_4	26	GPIO15	PD	8mA	GP Input	GP Output	PWM_TOUT_5	–	–	–
XPWMTOUT_5	25	GPIO16	PD	8mA	GP Input	GP Output	PWM_TOUT_6	–	–	–

UART Interface

Table 8. UART Interface

Pad Name & Default Funtion	Pad Number	GPIO Name	PU/PD	GPIO Drive	Option 1	Option 2	Option 3	Option 4	Option 5	Option 6
XUART0_RXD	21	GPIO52	PD	8mA	GP Input	GP Output	UART_0_RXD	–	–	–
XUART0_TXD	22	GPIO53	PD	8mA	GP Input	GP Output	UART_0_TXD	–	–	–
XUART1_RXD	39	GPIO04	PD	8mA	GP Input	GP Output	UART_1_RXD	UART_2_CTSn	–	–
XUART1_TXD	40	GPIO05	PD	8mA	GP Input	GP Output	UART_1_TXD	UART_2_RTSn	–	–
XUART2_RXD	41	GPIO06	PD	8mA	GP Input	GP Output	UART_2_RXD	–	–	–
XUART2_TXD	42	GPIO07	PD	8mA	GP Input	GP Output	UART_2_TXD	–	–	–
XUART3_RXD	44	GPIO08	PD	8mA	GP Input	GP Output	UART_3_RXD	–	–	–
XUART3_TXD	45	GPIO09	PD	8mA	GP Input	GP Output	UART_3_TXD	–	–	–

Debug Interface

Table 9. Debug Interface

Pad Name & Default Function	Pad Number	GPIO Name	PU/PD	GPIO Drive	Option 1	Option 2	Option 3	Option 4	Option 5	Option 6
XJTAG_TCK	11	–	PD	–	–	–	–	–	–	–
XJTAG_TMS	10	–	PU	–	–	–	–	–	–	–
XJTAG_TDI	13	–	PU	–	–	–	–	–	–	–
XJTAG_TDO	12	–	PD	–	–	–	–	–	–	–
XJTAG_TRST_N	9	–	PD	–	–	–	–	–	–	–
XDEBUG_RXD	23	–	PD	8mA	GP Input	GP Output	Xdebug_RXD	–	–	–
XDEBUG_TXD	24	–	PD	8mA	GP Input	GP Output	Xdebug_TXD	–	–	–

INT Interface

Table 10. Interrupt Interface

Pad Name & Default Function	Pad Number	GPIO Name	PU/PD	GPIO Drive	Option 1	Option 2	Option 3	Option 4	Option 5	Option 6
XEINT_0	14	GPIO45	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPA0[0]
XEINT_1	16	GPIO46	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPA0[1]
XEINT_2	15	GPIO47	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPA0[2]
XGPIO8	49	GPIO25	PD	2mA	GP Input	GP Output	SPI_3_CLK	–	–	NWEINT_GPG1[0]
XGPIO9	47	GPIO26	PD	2mA	GP Input	GP Output	SPI_3_CSn	–	–	NWEINT_GPG1[1]
XGPIO10	50	GPIO27	PD	2mA	GP Input	GP Output	SPI_3_MISO	–	–	NWEINT_GPG1[2]
XGPIO11	48	GPIO28	PD	2mA	GP Input	GP Output	SPI_3_MOSI	–	–	NWEINT_GPG1[3]
XGPIO12	46	GPIO29	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG1[4]
XGPIO13	72	GPIO30	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG1[5]
XGPIO14	73	GPIO31	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG1[6]
XGPIO15	69	GPIO32	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG1[7]
XGPIO16	70	GPIO33	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[0]
XGPIO17	71	GPIO34	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[1]
XGPIO18	65	GPIO35	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[2]
XGPIO19	66	GPIO36	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[3]
XGPIO20	67	GPIO37	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[4]
XGPIO21	68	GPIO38	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[5]
XGPIO22	6	GPIO39	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[6]
XGPIO23	7	GPIO40	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[7]

Reset Interface

Table 11. Reset Interface

Pad Name	Pad Number
XRESET_N	8

Power Interface

Table 12. Power Interface

Pad Name	Pad Number
VIN_3P3	[27-28]
GND	[1, 32, 43, 74, 75, 76, 77, 78, 79, 80, 81, 82]

ELECTRICAL SPECIFICATIONS

Absolute Maximum Rating

Table 13. Absolute Maximum Ratings

PAD Number	Symbol	Description	Min	Typ	Max	Units
[27, 28]	V_{IN}	Input voltage V_{IN}	–	–	3.8	V
[2-20], [23-26], [29-31], [33-42], [44-73]	$V_{undershoot}$	Undershoot voltage for I/O	-0.3	–	–	V
–	T_A	Storage Temperature	–40		85	°C

Recommended Operating Conditions

The recommended operation of the ARTIK 055s Module is based on the operating conditions listed in *Table 14*

Table 14. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Main Power Supply: PAD: [27, 28]	VIN_3P3	3.1	3.3	3.6	V
Operating Temperature	T_c	-20	–	85	°C

DC Electrical Characteristics

Table 15. GPIO DC Electrical Characteristics

PAD Number	Symbol	Description	Condition		Min	Typ	Max	Units
[6-7], [14-26], [29-31], [33-42], [44-73]	V_{TOL}	Tolerant External Voltage	3.3 Power Off and On		–	–	3.6	V
	V_{IH}	High-Level Input Voltage						
		CMOS Interface	–		2.31	–	3.6	V
	V_{IL}	Low-Level Input Voltage						
		CMOS Interface	V_{DD} = 3.3V ± 10%		-0.3	–	0.7	V
	Δ_V	Hysteresis Voltage	–		0.15	–	–	V
	I_{IH}	High-Level Input Current						
		Input Buffer	V_{IN} = 3.3V	V_{DD} = 3.3V Power On	-3	–	3	µA
				V_{DD}= 3.3V Power Off & SNS=0	-5	–	5	
		Input Buffer Pull-Down	V_{IN} = 3.3V	V_{DD} = 3.3V ± 10%	13	40	90	
	I_{IL}	Low-Level Input Current						
		Input Buffer	V_{IN} = 0V	V_{DD} = 3.3V Power On and Off	-3	–	3	µA
		Input Buffer Pull-Down	V_{IN} = 0V	V_{DD} = 3.3V	-13	–	-90	
	V_{OH}	Output High Voltage	I_{OH} = 2.0mA, 4.0mA, 8.0mA and 12.0mA		2.64	–	3.3	V
	V_{OL}	Output Low Voltage	I_{OL} = -2.0mA, -4.0mA, -8.0mA and -12.0mA		0	–	0.66	
	V_{OZ}	Output Hi-Z Current	–		-5	–	5	µA
	C_{IN}	Input Capacitance	Any input and bi-directional buffers		–	–	5	pF
	C_{OUT}	Output Capacitance	Any output buffers		–	–	5	pF

Table 16. GPIO Signal Drive Strengths

State	Currents: Max conditions V_{DD} = 3.3V	Units
0	2	mA
1	4	mA
2	8 (default)	mA
3	12	mA

Table 17. ADC DC Electrical Characteristics

PAD Number	Symbol	Description	Condition	Min	Typ	Max	Units
[2-5]	V_{IH}	High Level Input Voltage	Guaranteed Logic High Level	1.26	–	1.8	V
	V_{IL}	Low Level Input Voltage	Guaranteed Logic Low Level	0	–	0.54	V
	V_{OH}	Output High Voltage	I_{OH} = 2mA, 4mA, 8mA and 12mA	1.44	–	1.8	V
	V_{OL}	Output Low Voltage	I_{OL} = 2mA, 4mA, 8mA and 12mA	0	–	0.36	V
	I_{RPU}	Input Pull-Up Resistor Current	V_{PAD} = 0	15	–	77	µA
	I_{RPD}	Input Pull-Down Resistor Current	V_{PAD} = 1.8	17	–	77	µA
	V_H	Input Hysteresis	–	0.18	–	–	V
	I_{PAD}	Input Leakage Current for Non Tolerant Cells	D_{VDD} = 1.8, V_{PAD} = 0 or 1.8V	-6	–	+6	µA
	I_{OZ}	Off State Leakage Current	D_{VDD} = 1.8, V_{PAD} = 0 or 1.8V	-6	–	+6	µA

Power and Current Consumption

The values in this table are nominal. Measurements were taken on sample boards at room temperature using a 3.3V system power supply.

Table 18. ARTIK 055s Module Power Consumption

Category	Scenario	Condition	Throughput Conditions	Current (mA)	Power (W)
Wi-Fi	802.11n Tx	Transfer packet using iperf3 @ 25 Mbps	Max	320	1.06
	802.11n Rx	Transfer packet using iperf3 @ 25 Mbps	Max	240	0.79
	802.11n Idle	DTIM3	–	54	0.18

ESD Ratings

RF Electrical Characteristics

Table 19. ESD Ratings

Parameter	Min	Typ	Max	Units
ESD stress voltage Human Body Model (JEDEC)	-1.0	–	1.0	kV
ESD stress voltage Charged Device Model	–	250	–	V

Table 20. Tx Performance Characteristics

Parameter	Min	Typ	Max	Units
RF frequency range	2412	-	2472	GHz
11b (1-11Mbps)	–	16	–	dBm

Table 20. Tx Performance Characteristics

Parameter	Min	Typ	Max	Units
11g (6-54Mbps)	–	13	–	dBm
11n, HT20 (MCS0-7)	–	12	–	dBm

Table 21. Rx Performance Characteristics [a]

Parameter	Min	Type	Max	Units
RF frequency range	2412	–	2472	GHz
11b (1Mbps)	–	–96	–	dBm
11b (11Mbps)	–	–87	–	dBm
11g (6Mbps)	–	–91	–	dBm
11g (54Mbps)	–	–74	–	dBm
11n, HT20 (MCS0)	–	–92	–	dBm
11n, HT20 (MCS07)	–	–71	–	dBm

a. Measured in a conduction test performed in a shielded room

MECHANICAL SPECIFICATIONS

Figure 5 shows the mechanical dimensions of the ARTIK 055s Module. All dimensions are in mm.

NOTE

The top layer "NO PCB ROUTING" gray areas are to prevent any shorts between exposed vias or traces and unused ARTIK 055s Module pads.

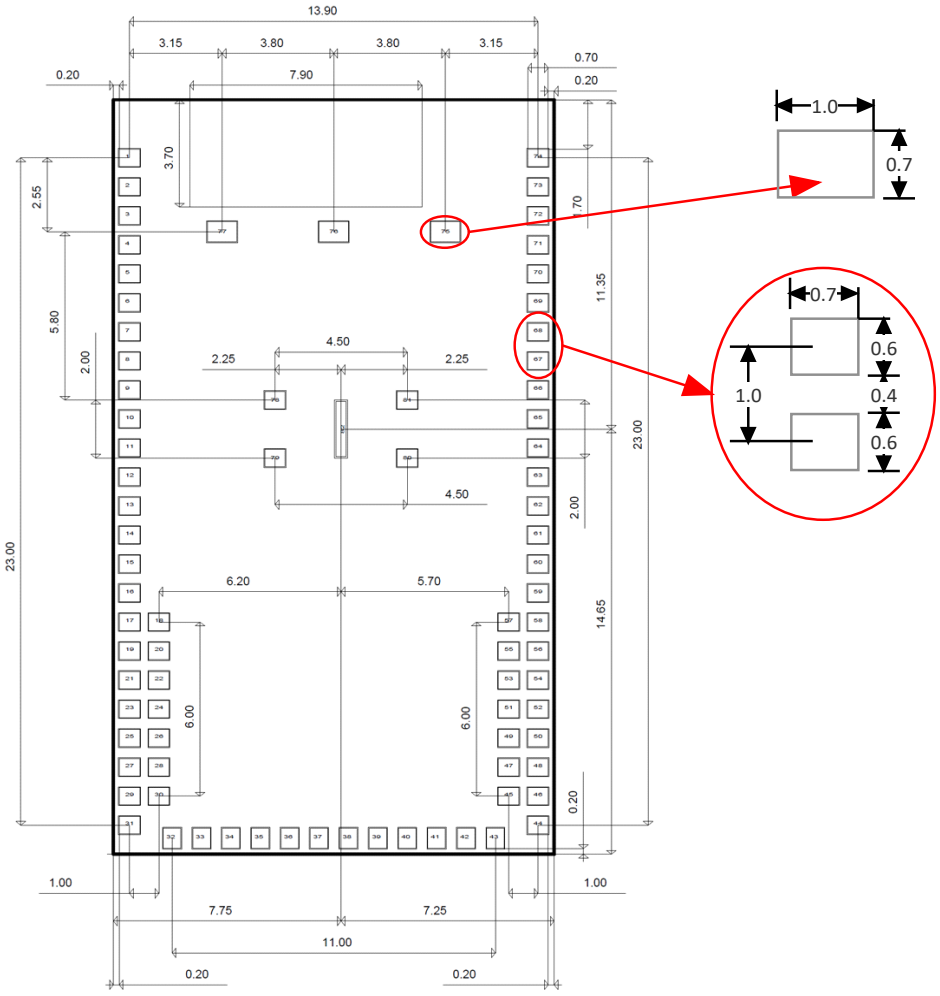


Figure 5. ARTIK 055s Module Mechanical Dimensions (Top View)

NOTE

The ground pads (79–82) are *not* centered on the module.

Module Antenna Placement Requirements

The ARTIK 055s Module has an integrated on-module antenna. The figure below describes the required restrictions on location when placing the ARTIK 055s Module on your native PCB design. In addition, adhere to the following guidelines:

- To avoid severe Wi-Fi radiation loss, Samsung Semiconductor, Inc. strongly recommends allocating a “No PCB Routing or Power Planes” metal-free area of at least 7.9×3.7mm in the Wi-Fi Antenna keep-out area underneath the module, and component keep-out areas of 5×6.7mm (all layers) next to the on-module antenna, as shown in *Figure 6*.
- Locate the antenna area at the edge of your PCB board, and as far away from other electronics as possible.

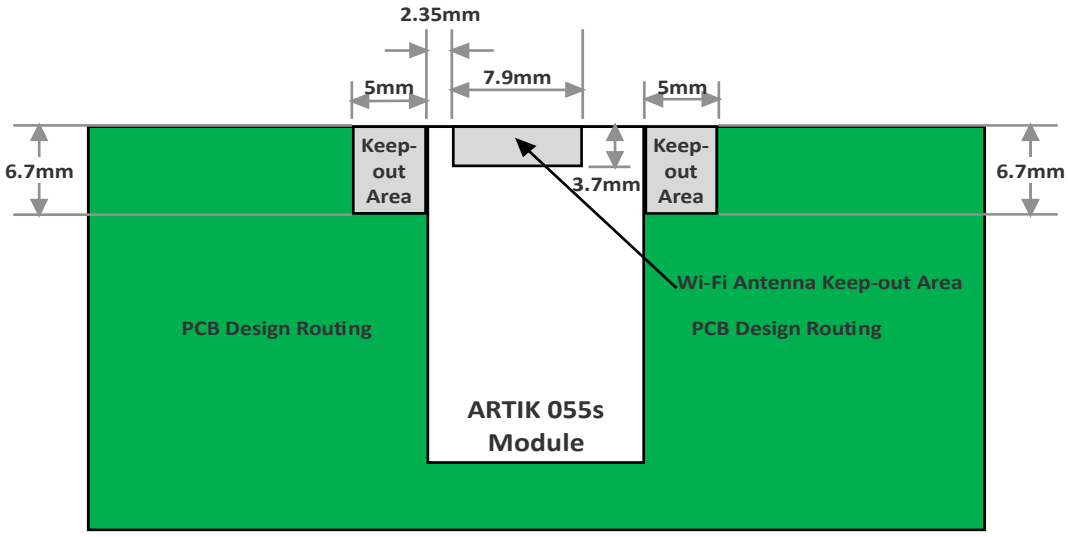


Figure 6. Module Placement Restrictions

CERTIFICATION AND COMPLIANCE

CE

The ARTIK 055s Module is in compliance with each applicable article of the Radio Equipment Directive (RED) Compliance with the following standards was confirmed:

- Article 3.1a (Health and Safety) EN 60950-1:2006 + A11:2009 + A1:2010 + A12:2001 + A2:2013
- Article 3.1.b (EMC) EN 301 489-1 V2.1.1
  EN 301 489-17 V3.1.1
- Article 3.2 (Radio spectrum use) EN 300 328 V2.1.1
  EN 62311:2008

For a formal notified body statement of opinion contact your sales representative.

FCC Regulatory Disclosures

This device complies with Part 15 of the FCC`s Rules. Operation is subject to the following two Conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesirable operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/ TV technician for help.

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with a minimum distance of 20cm between the transmitter's radiating structure(s) and the body of the user or nearby persons.

This module is intended for OEM integration. The OEM integrator is responsible for FCC compliance and compliance with all applicable regulations including those for modular transmitters 47 C.F.R. 15.212. The OEM product must comply with all applicable labeling requirements including those contained in 15 C.F.R. 15.19. The OEM is solely responsible for certification and testing and labeling of its own products. In addition to any independently required labels, the OEM shall also affix to the outside of a device into which the module is installed a label referring to the enclosed module. This exterior label should be prepared in a legible font and permanently affixed and using the wording "Contains Transmitter Module FCCID: A3LSIP0P5WRS50."

The OEM is required to ensure that the end product integrates this module so as to maintain a minimum distance of 20 cm between the equipment's radiating structure(s) and the body of the user or nearby persons. The OEM shall also advise its end user of this requirement as required by applicable rules.

The OEM shall require that the end user of its product be informed that the FCC radio frequency exposure guidelines for an uncontrolled environment can be satisfied. The OEM shall further inform its end user that any change or modifications to this module not expressly approved by the manufacturer will void the warranty and the users' authority to operate the equipment.

Wi-Fi

The ARTIK 055s Module is recognized as Wi-Fi CERTIFIED™ by the Wi-Fi Alliance®:

Classification	Program
Connectivity	Wi-Fi CERTIFIED b, g, n
	WPA™ - Personal
	WPA2™ - Personal
Optimization	WMM®

Certification ID: WFA75217.

Industry Canada Regulatory Disclosures

Industry Canada Statement

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Cet appareil est conforme avec Industrie Canada exempts de licence standard RSS (s). L'opération est soumise aux deux conditions suivantes:(1) cet appareil ne peut causer d'interférences, et?(2) cet appareil doit accepter toute interférence, y compris les interférences qui peuvent causer un mauvais fonctionnement de l'appareil.

Industry Canada Radiation Exposures Statement and Limitations on Use

This equipment complies with IC RSS-102 radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator and your body. This equipment should be installed and must not be co-located or operating in conjunction with any other antenna or transmitter.

In the United States and Canada, only Channel 1~11 can be operated and these channel assignments deal only with the 2.4 GHz range.

The end product must be labeled to display the Industry Canada certification number of the module

Contains transmitter module IC: 649E-SIP0P5WRS50

Le dispositif d'accueil doivent être étiquetés pour afficher le numéro de certification d'Industrie Canada du module.

Contient module émetteur IC : 649E-SIP0P5WRS50

KC

The ARTIK 055s Module complies with the standards set by the Korean communications commission (KC).

KC Identifier: MSIP-CRM-SEC-SIP0P5WRS50

SRRC

Both the ARTIK 055s Module complies with the standards set by the People's Republic of China.

CMIIT ID: 2017DJ7910

EU Regulatory Disclosures

CE Statement

The following statement must be supplied with each product but can be printed in the user manual, the packaging, or provided as a separated leaflet.

> Hereby, Samsung declares that this IoT Module is in compliance with the essential requirements and other relevant provisions of Article 3 Essential requirements of the Radio Equipment Directive 2014/53/EU and RoHS directive 2011/65/EU.
>
> "The declaration of conformity may be consulted at www.artik.io/certification"

The OEM is required to ensure that the end product integrates this module so as to maintain a minimum distance of 20 cm between the equipment's radiating structure(s) and the body of the user or nearby persons. The OEM shall also advise its end user of this requirement as required by applicable rules.

Ordering Information

Type	Order Number	Description
ARTIK 055s Module	SIP-0P5WRS502	One ARTIK 055s Module
ARTIK 055s Development Kit	SIP-KITNXH002	One ARTIK 055s Module One Embedded Evaluation Board

For volume ordering of evaluation kits, contact a sales representative in your area or visit:

https://www.artik.io/contact-us/

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